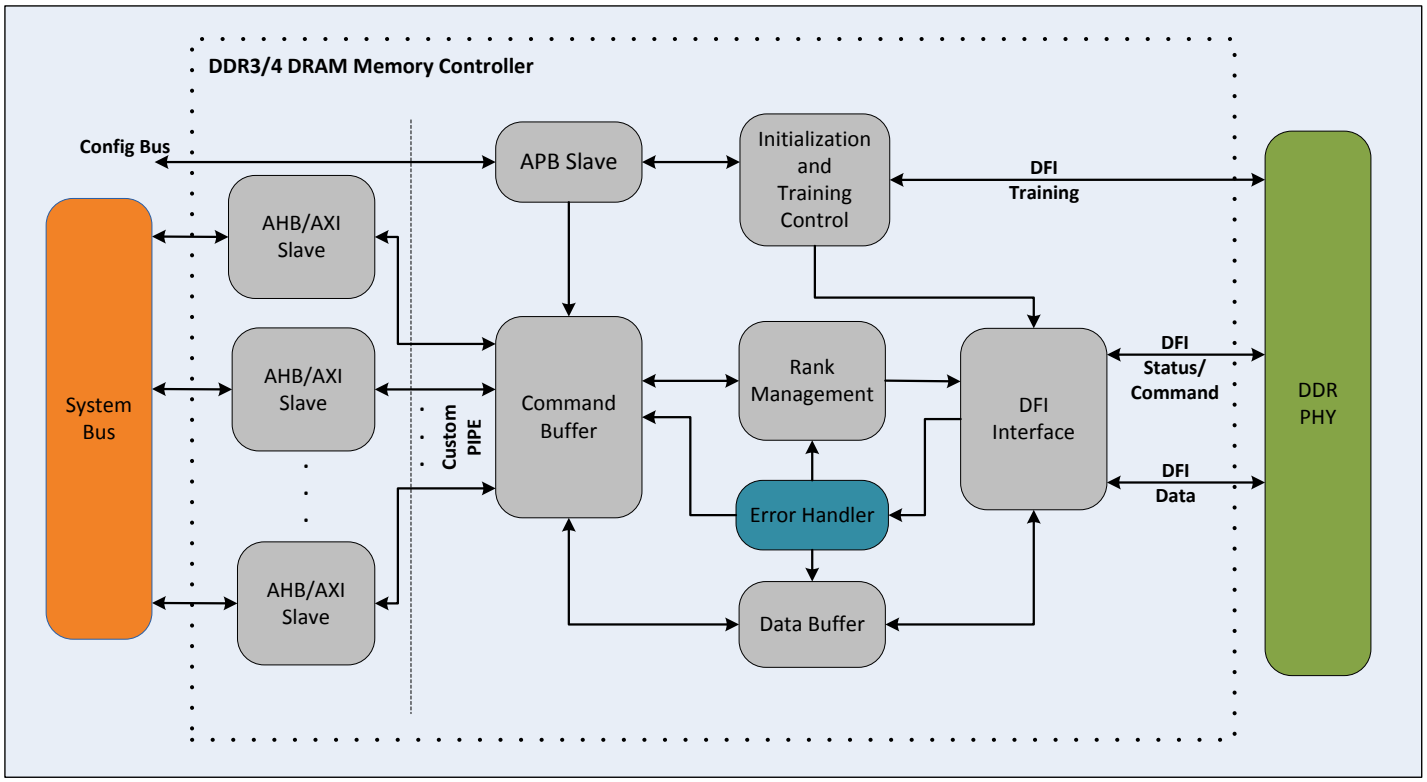
DDR3/4 DRAM Memory Controller

SoC companies are faced with a challenge during the early stage of chip design to choose between DDR3 and DDR4, as they are skeptic about their performance requirements. We, at Arastu, have developed a DDR3/4 DRAM Memory Single Controller, which gives designers the flexibility to choose DRAM memories that fits best into their needs. The hardware for the controller is generated based on the parameters configured by the user. The design IP supports the industry standard AHB/AXI, however, can be customized as per customer's requirement. It is optimized for ASIC and FPGA designs.

Block Diagram:



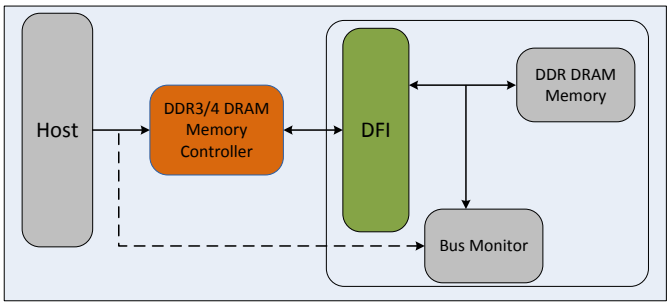
Note: The color "Blue" in the figure above depicts CRC/Parity error handling function - ***(specific to DDR4)***

Feature Highlights:

- Fully compliant with JEDEC standard JESD79-3F & JESD79-4A for DDR3 and DDR4 respectively
- Fully compliant with DFI3.1 PHY specifications
- Supports all DDR3/4 commands and trainings
- BL8 and On-the-fly (BL8/BC4) programmable burst lengths
- Data Bus Inversion (DBI) - (***specific to DDR4***)
- Supports Data Mask (DM)
- Multiple Power Down modes
- Low Power Auto Self Refresh (LPASR) support
- Supports upto eight ranks
- Parameterized rank data widths 8, 16, 32, 64
- Upto 8 and 16 banks per chip support for DDR3 and DDR4 respectively
- Supports upto 32 Gbit chips with x4/x8/x16 data ports
- Software driven Mode Register (MR) Write and Mode Page Read/Write
- Full runtime configurable timing parameters and memory settings
- Supports chip select interleaving
- Registered Dual In-line Memory Module (RDIMM) and Load Reduced DIMM (LR-DIMM) support
- ODT, dynamic ODT and write leveling calibration

- Parameterized request queue depth
- QoS through various arbitration schemes
- User-customizable arbiter
- Supports Intelligent request scheduling
- Software driven controlled frequency change
- Supports maskable interrupt generation
- Automated DRAM Initialization
- Supports Per-DRAM Addressability - (***specific to DDR4***)
- DDR4 3DS device configurations support - (***specific to DDR4***)

Usage Model:



Additional Aspects:

- Supports 1:1, 1:2 and 1:4 MC to PHY frequency ratio
- Error Correction Code (ECC) Generation/Checking
- Supports CRC computation across the data bus for error detection - (***specific to DDR4***)
- Supports Parity generation for command/address bus to verify the integrity - (***specific to DDR4***)
- Seamless error recovery in case of CRC/Parity error - (***specific to DDR4***)
- Maximizes DRAM bus utilization by implementing Look-Ahead command processing, Bank Management, Auto-Precharge
- Highly intelligent scheduler that includes multiple algorithms to improve the memory throughput
- Programmable to achieve minimal latency for a given application

Value Proposition:

- Read Modify Write (RMW) - (Optional)
- Row Hammering Detection (RHD) from data pattern - (Optional)
- Software driver Post Package Repair and Target Row Refresh - (Optional)
- Supports multiple host buses AMBA AXI4, AHB, Custom PIPE based Interface with parameterized address/data widths - (Optional)
- Valuable add-on cores such as AHB/AXI, Multi-port Frontend and Reorder core available - (Optional)
- Optimized for minimum ASIC gate count
- Flexible licensing models
- Customization and Integration services
- Expert Technical support with maintenance updates

Applications:

- Computers and Gaming Consoles
- Data Center and Server Market
- Enterprise applications such as communication and networking
- High-Performance Computing
- Data Processing

Deliverables:

- Synthesizable Source code
- SDC & UPF Constraint details
- UserGuide and Release notes
- Examples' showing how to connect and usage of the Controller
- Verification Components available upon request