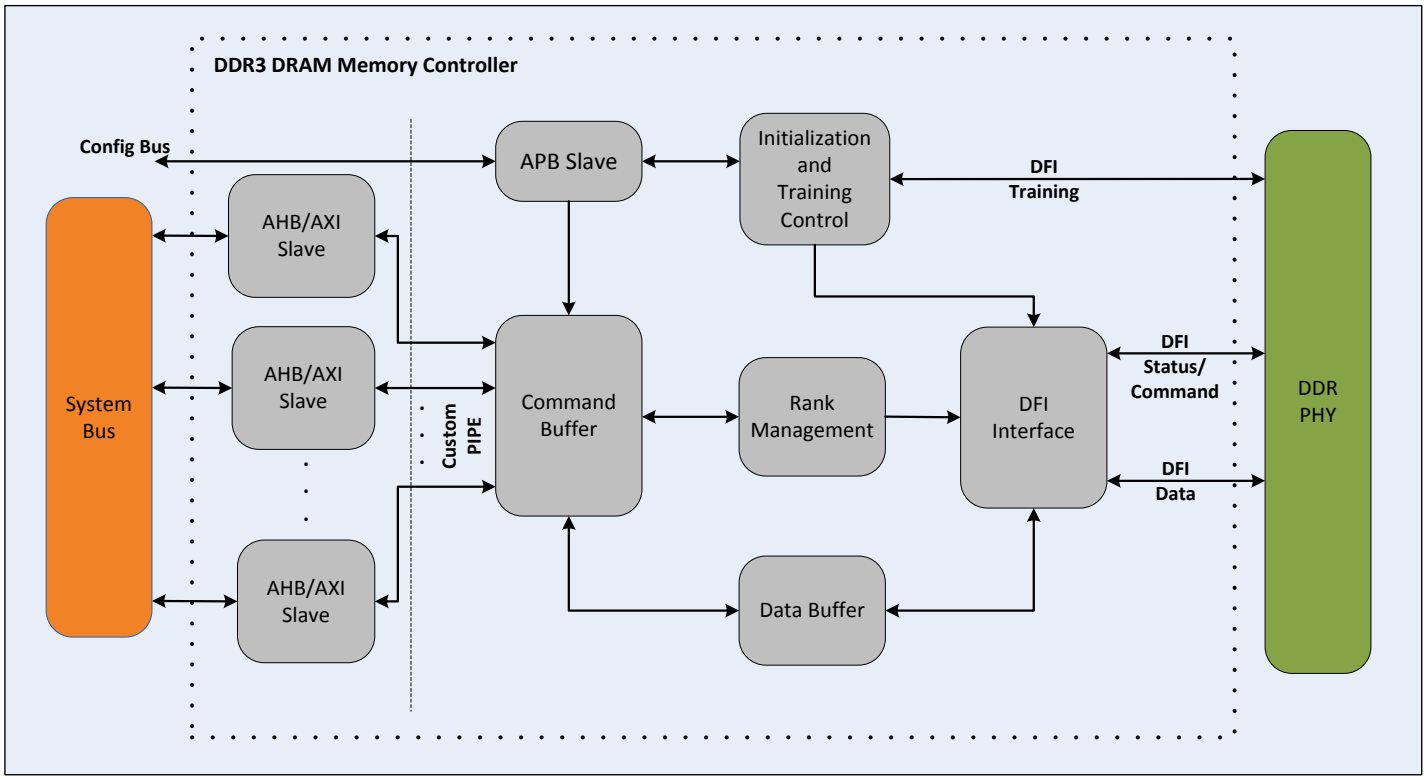
DDR3 DRAM Memory Controller

DDR3's capability to bolster performance in system devices for a large number of applications have made it to be a widely accepted and established DRAM memory in the industry today. Considering the demand, we at Arastu, have developed a robust and flexible DDR3 DRAM Memory Controller IP and target to make the integration of DDR3 into your SoC a smooth one. The design IP supports the industry standard AHB/AXI, however, can be customized as per customer's requirement. The controller is fully optimized for ASIC and FPGA designs.

Block Diagram:



Feature Highlights:

- Fully compliant with JEDEC standard JESD79-3F and DFI3.1 PHY specifications
- Supports all DDR3 commands and trainings
- BL8 and On-the-fly (BL8/BC4) programmable burst lengths
- Write Data Mask (DM) support
- Supports multiple Power Down modes
- Low Power Auto Self Refresh (LPASR)
- Supports upto eight ranks
- Parameterized rank data widths 8, 16, 32, 64
- Upto 8 banks per chip support
- Supports upto 8 Gbit chips with x4/x8/x16 data ports
- Software driven Mode Register (MR) Write and Mode Page Read/Write
- Full runtime configurable timing parameters and memory settings
- Chip select interleaving
- Registered Dual In-line Memory Module (RDIMM) and Load Reduced DIMM (LR-DIMM)
- ODT, dynamic ODT and write leveling calibration
- Parameterized request queue depth
- QoS through various arbitration schemes
- User-customizable arbiter
- Supports Intelligent request scheduling
- Software driven controlled frequency change
- Supports maskable interrupt generation
- Automated DRAM Initialization

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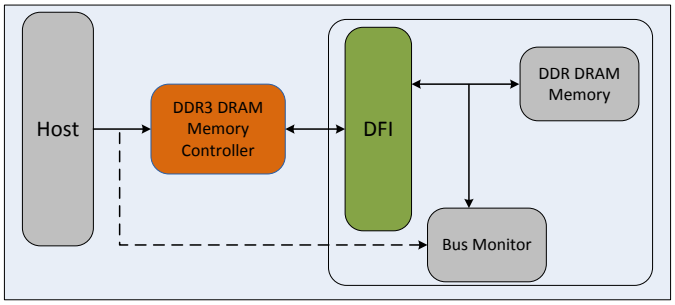
Usage Model:



Additional Aspects:

- Supports 1:1 and 1:2 MC to PHY frequency ratio
- Error Correction Code (ECC) Generation/Checking - (Optional)
- Maximizes DRAM bus utilization by implementing Look-Ahead command processing, Bank Management, Auto-Precharge
- Highly intelligent scheduler that includes multiple algorithms to improve memory throughput
- Programmable to achieve minimal latency for a given application

Applications:

- Data Processing applications such as streaming media devices utilizes DDR3, as it can provide significant performance boost
- DDR3 is highly reliable and therefore can be utilized in harsh environments such as Defense technology
- Supports High-Performance Computing SoC's in Avionics, UAV's, Missile Systems

Value Proposition:

- Read Modify Write (RMW) - (Optional)
- Support for Row Hammering Detection (RHD) from data pattern - (Optional)
- Software driver Post Package Repair and Target Row Refresh - (Optional)
- Supports multiple host buses AMBA AXI4, AHB, Custom PIPE based Interface with parameterized address/data widths
- Valuable add-on cores such as AHB/AXI, Multi-port Frontend and Reorder core available - (Optional)
- Optimized for minimum ASIC gate count
- Flexible licensing models
- Customization and Integration services
- Expert Technical support with maintenance updates

Deliverables:

- Synthesizable Source code
- SDC & UPF Constraint details
- UserGuide and Release notes
- Examples' showing how to connect and usage of the Controller
- Verification Components available upon request