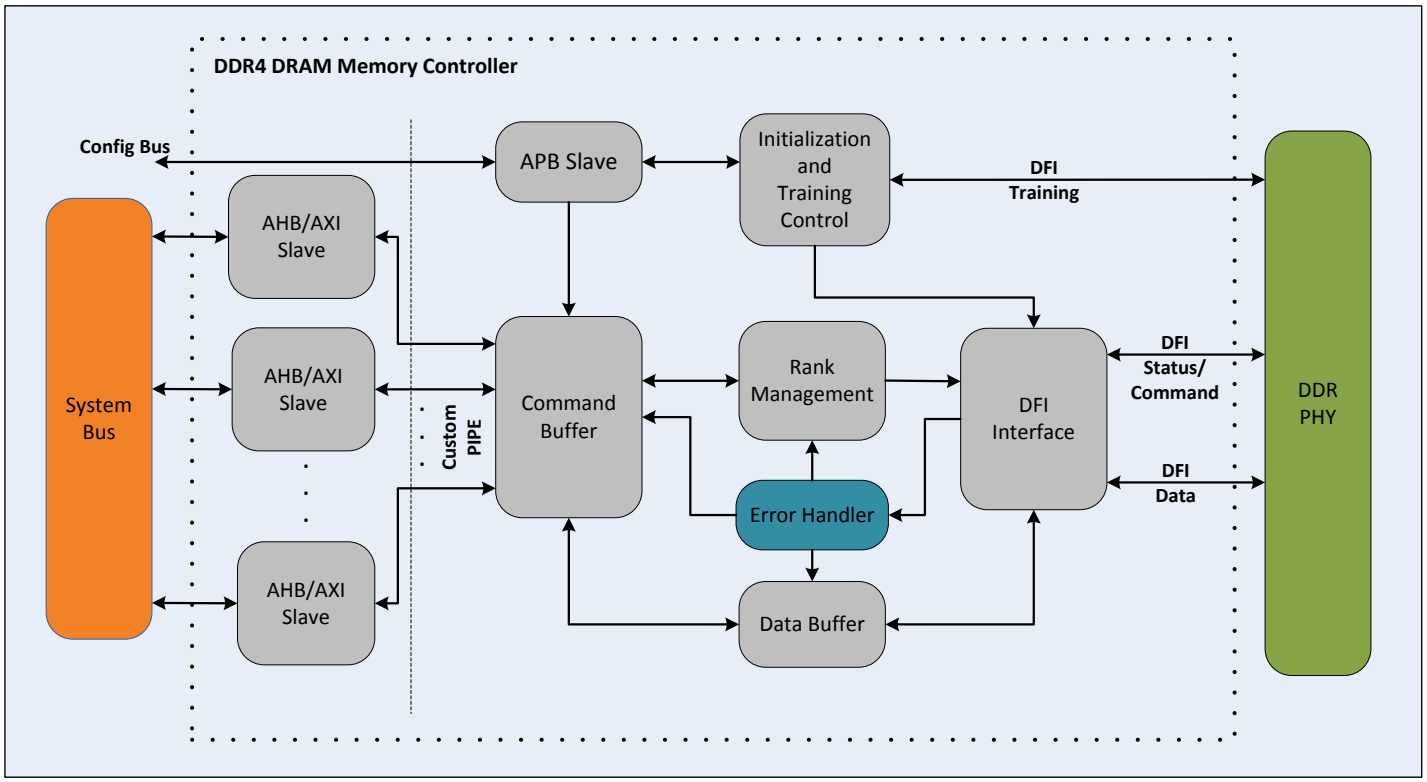
# DDR4 DRAM Memory Controller

DDR4 DRAM is no longer the memory only for Laptops and Servers, its ability to deliver increased performance and be highly reliable has led to its demand and adoption in multiple domains. At Arastu, we have developed a robust and flexible DDR4 DRAM Memory Controller IP and target to make the integration of DDR4 into your SoC a smooth one. The Design IP supports the popular industry standard AHB/AXI master, however, can be customized as per customer's requirement. The controller is optimized for ASIC and FPGA designs.

## Block Diagram:




## Feature Highlights:

- Fully compliant with JEDEC standard JESD79-4A and DFI3.1 PHY specifications
- Supports all DDR4 commands and trainings
- BL8 and On-the-fly (BL8/BC4) programmable burst lengths
- Data Bus Inversion (DBI) and Data Mask (DM)
- Low Power Auto Self Refresh (LPASR)
- Multiple Power Down modes
- Supports upto eight ranks
- Parameterized rank data widths 8, 16, 32, 64
- Upto 16 banks per chip support
- Scheduling Traffic for Efficient Bank Group(BG) Use
- Supports upto 32Gbit chip with x4/x8/x16 data ports
- Software driven Mode Register(MR) Write, Mode Page Read/Write, PDE(X), DES, SRE
- Full runtime configurable timing parameters and memory settings
- Supports chip select interleaving
- Registered Dual In-line Memory Module (RDIMM) and Load Reduced DIMM (LR-DIMM)
- ODT, dynamic ODT and write leveling calibration
- Parameterized request queue depth
- QoS through various arbitration schemes
- User-customizable arbiter
- Intelligent request scheduling
- Software driven controlled frequency change
- Supports maskable interrupt generation
- Automated DRAM Initialization
- Supports Per-DRAM Addressability
- DDR4 3DS device configurations support

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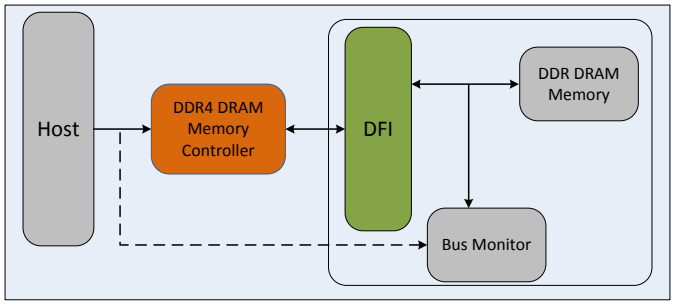
## Usage Model:




## Additional Aspects:

- Supports 1:1, 1:2 and 1:4 MC to PHY frequency ratio
- Error Correction Code (ECC) Generation/Checking
- Supports CRC computation across the data bus for error detection
- Supports Parity generation for command/address bus to verify the integrity
- Seamless error recovery in case of CRC/Parity error
- Maximizes DRAM bus utilization by implementing Look-Ahead command processing, Bank Management, Auto-Precharge
- Highly intelligent scheduler that includes multiple algorithms to improve the memory throughput
- Programmable to achieve minimal latency for a given application

## Value Proposition:

- Read Modify Write (RMW) - (Optional)
- Support for Row Hammering Detection (RHD) from data pattern - (Optional)
- Software driver Post Package Repair and Target Row Refresh - (Optional)
- Supports multiple host buses AMBA AXI4, AHB, Custom PIPE based Interface with parameterized address/data widths - (Optional)
- Valuable add-on cores such as AHB/AXI, Multi-port Frontend and Reorder core available - (Optional)
- Optimized for minimum ASIC gate count
- Flexible licensing models
- Customization and Integration services
- Expert Technical support with maintenance updates

## Applications:

- Increased Performance for Data Centers and Enterprises
- Reduces standby power by 40-50% in contrast to predecessors for consumer devices such as laptops, smartphones etc.

## Deliverables:

- Synthesizable Source code
- SDC & UPF Constraint details
- UserGuide and Release notes
- Examples' showing how to connect and usage of the Controller
- Verification Components available upon request