Ethernet 10G Switch IP Core

Arastu System's **Ethernet 10G Switch IP Core** is designed to fit into today's FPGA and ASIC technologies with low gate count. The core can be easily configured to support multiple speed ports with fully non-blocking switching. The architecture is an optimized cut-through design which enables sub-100ns port-to-port latency.

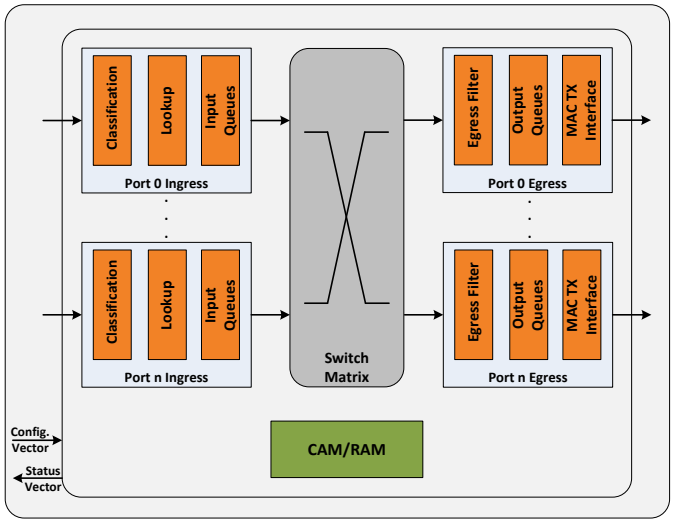
Feature Highlights:

- Highly configurable and low latency
- Configurable number of ports maximum ***up to 24***
- Each port can be either ***10M/100M/1G/2.5G/10G***
- Cut-through, non-blocking architecture
- Virtual Output Queuing which prevents Head-of-Line blocking
- Configurable Queue sizes
- Synthesizable content-addressable memory ***(CAM)*** for fast lookup
- ***RAM*** based lookup to support up to 4K MAC addresses
- Configurable number of MAC address entries
- Automated lookup table learning and aging with lockable entries
- VLAN support
- QoS priority switching and Configurable number of priority queues
- Priority flow control based on 802.1Q
- Support for Jumbo and Super Jumbo frames
- Port mirroring and loopback
- Software based Multi-cast grouping
- Unmanaged ***Layer2+ switching***
- Optional control interface for managed switch and diagnostic access
- Support for Xilinx Virtex-6, Kintex-7 and Virtex-7 FPGA's
- Altera Stratix 4 and Stratix 5 FPGA support
- Support for 130nm and below ASIC's

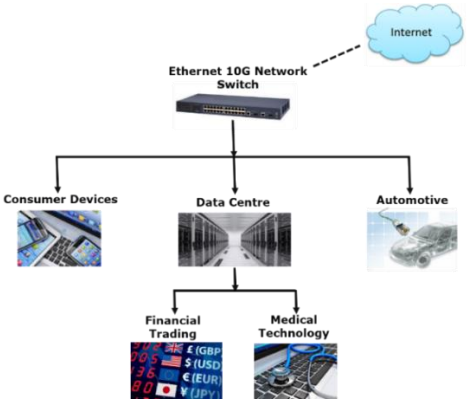
Value Proposition:

- Can be customized as per design requirements
- Privilege to run at ***156MHz*** with a 64-bit datapath or ***312MHz*** with a 32-bit datapath
- Precision time protocol (PTP) ***1588*** – (Optional)
- Flexible licensing models
- Customization and Integration services

Block Diagram:



Usage Model:



Applications:

- Low latency embedded markets for custom switching
- Provides low cost solutions for SMB (Small and Medium sized Business) market
- Replace ASSP's (Application Specific Standard Product) in wireless backhaul applications

Deliverables:

- SystemVerilog Source code and Verification environment
- SDC Compiler Constraints
- UserGuide and Release notes
- Examples' showing how to connect and usage of the IP Core