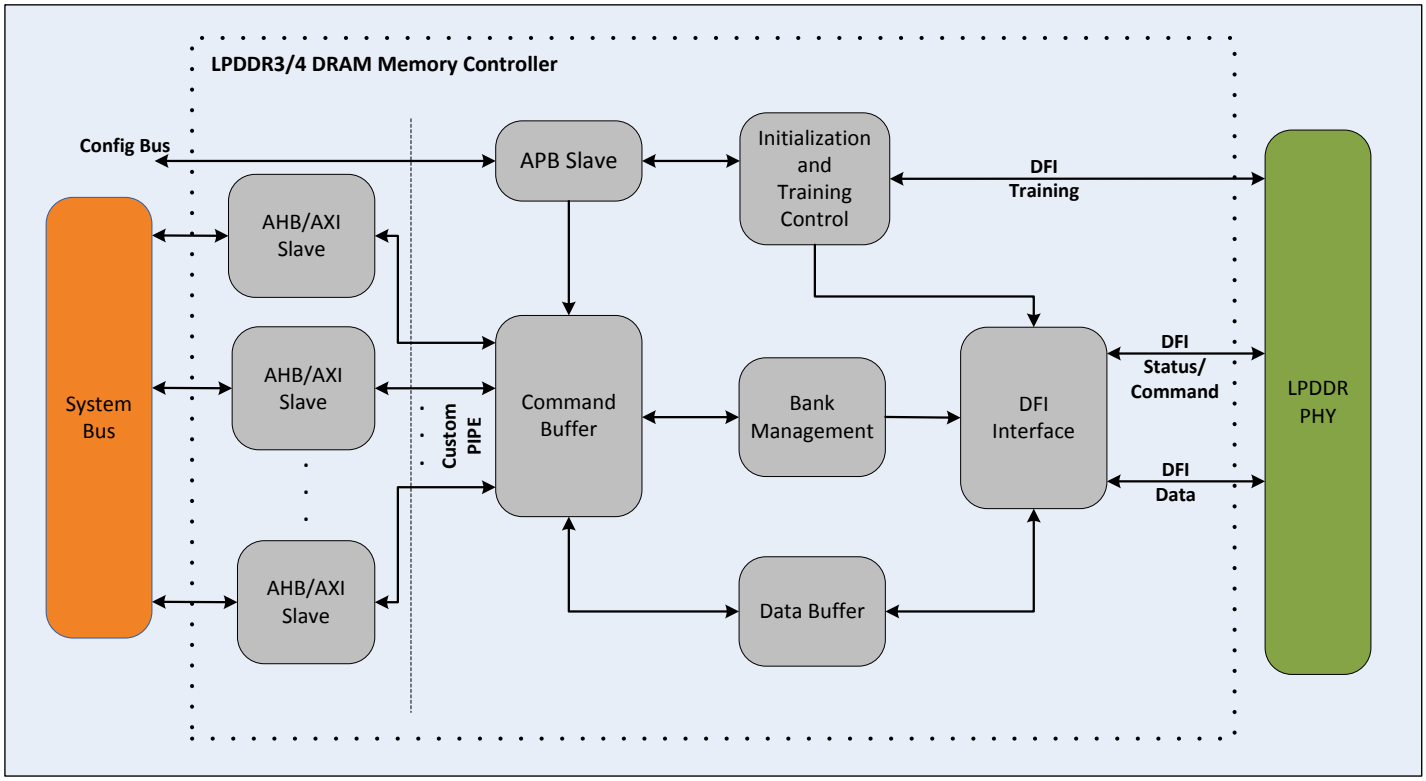
LPDDR3/4 DRAM Memory Controller

High-end computing applications require Higher Performance keeping the Power and Latency intact. On customer demand, after successful implementation of LPDDR4 Memory Controller, Arastu Systems have developed a LPDDR3/4 DRAM Memory Controller in order to support wide range of application using the same design. The design IP supports the industry standard AHB/AXI, however, can be customized as per customer's requirement. The controller is optimized for ASIC and FPGA designs.

Block Diagram:



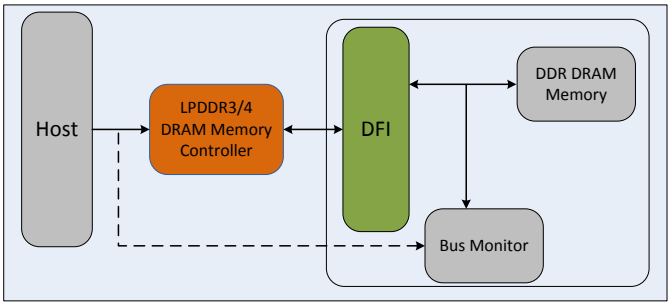
Feature Highlights:

- Fully compliant with JEDEC standard JESD209-3C and JESD209-4B
- Compliant with DFI3.1 and DFI4.0 PHY specifications
- Supports all LPDDR3/4 commands and trainings
- Configurable LPDDR DIMM Data Width
- Supports Multiple Ranks through parameter
- BL16 and On-the-fly (BL16/BL32) programmable burst lengths - ***(Specific to LPDDR4)***
- Support for BL8 read/write/mask-write commands - ***(Specific to LPDDR3)***
- Software driven Mode Register (MR) Read/Write
- Programmable READ/WRITE latency and related timings support
- Supports system byte addressing with uneven data strobe for LPDDR3 and Read Modify Write for LPDDR4
- Data Mask (DM)
- Data Bus Inversion (DBI) - ***(Specific to LPDDR4)***
- Software controlled frequency change with FSP-OP ***(Specific to LPDDR4)***
- Support Multiple frequencies
- Self-Refresh, Auto Refresh and per bank refresh
- Supports Self-Refresh Abort
- Self-Refresh Power Down (SRPD), Power Down mode and Clock Stop
- Deep Power Down mode - ***(Specific to LPDDR3)***
- Target Row Refresh (TRR) - ***(Optional)***
- Post Package Repair (PPR) - ***(Specific to LPDDR4)***

Additional Aspects:

- Supports 1:1, 1:2 and 1:4 MC to PHY frequency ratio
- Software driven runtime frequency change and power-down control
- Facilitates device temperature changes using configurable ReadInterval to modify Refresh rate
- Maximizes DRAM bus utilization by implementing Look-Ahead command processing and Bank Management
- Supports maskable interrupt generation
- Programmable to achieve minimal latency for a given application
- Full runtime configurable timing parameters and memory setting

Usage Model:



Value Proposition:

- Will be customized as per Customers' design requirements
- Customized System interface that fits into Customers' need
- Solution delivered completely integrated and validated with targeted PHY - ***(Optional)***
- Valuable add-on cores such as AHB/AXI, TRR, APB testbus available - ***(Optional)***
- Supports upto 8 system host interfaces
- Programmable Priority/QoS based system bus interface
- Optimized for minimum ASIC gate count
- Flexible licensing models
- Expert Technical support with maintenance updates

Applications:

- Consumer Gadgets such as Smartphone, Tablet, Ultrabook, Gaming Console, Personal Navigation System etc.
- Applications like ADAS (Advanced Driver Assistance Systems) and Infotainment Systems in the Automotive segment
- Graphic Processing market
- Patient Monitoring Devices and Portable Ultrasound machines in the Healthcare area

Deliverables:

- Synthesizable Source code
- SDC & UPF Constraint details
- UserGuide and Release notes
- Automatic Core maintenance updates
- Verification Components available upon request