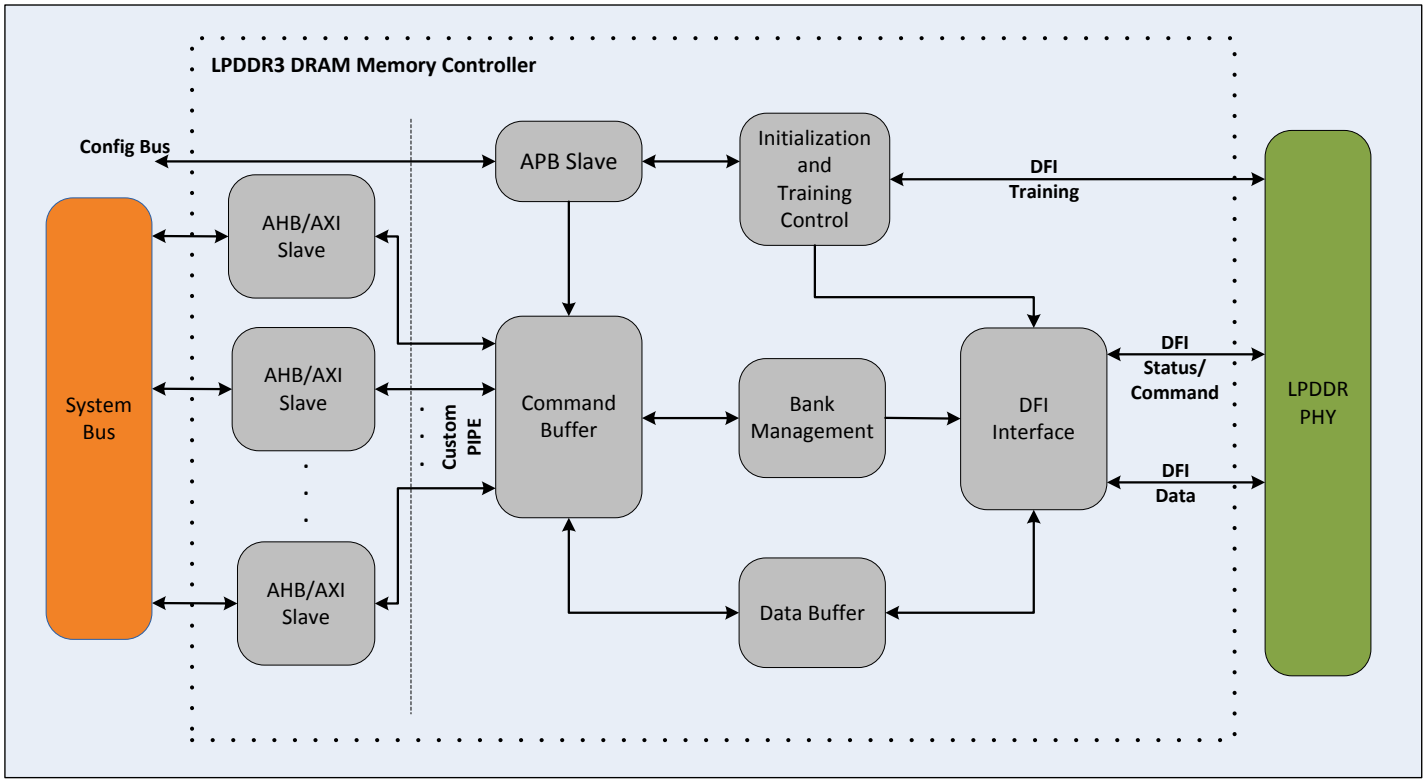
LPDDR3 DRAM Memory Controller

Increased Bandwidth, Low Power Consumption, Extended Battery Life are some of the advantages the LPDDR3 DRAM offers in contrast to predecessors. At Arastu, we have developed a highly flexible and configurable design for LPDDR3 DRAM Memory Controller. The design IP supports the industry standard AHB/AXI, however, can be customized as per customer's requirement. The controller is optimized for ASIC and FPGA designs.

Block Diagram:



Feature Highlights:

- Fully compliant with JEDEC standard JESD209-3C and DFI3.1 PHY specifications
- Supports all LPDDR3 commands and trainings
- Configurable LPDDR DIMM Data Width
- Supports Multiple Ranks through parameter
- Support for BL8 read/write/mask-write commands
- Software driven Mode Register (MR) Read/Write
- Programmable READ/WRITE latency and related timings support
- System byte addressing with uneven data strobe
- Supports Data Mask (DM)
- Supports Self-Refresh Abort
- Self-Refresh, Auto Refresh and per bank refresh
- Support Multiple frequencies
- Power Down and Deep Power Down modes
- Parameterized LPDDR3 data-width (x16/x32) configuration

Additional Aspects:

- Supports 1:1, 1:2 and 1:4 MC to PHY frequency ratio
- Software driven runtime frequency change and power-down control
- Facilitates device temperature changes using configurable ReadInterval to modify Refresh rate
- Maximizes DRAM bus utilization by implementing Look-Ahead command processing, Bank Management and Intelligent Request Scheduling
- Supports maskable interrupt generation
- Full runtime configurable timing parameters and memory settings

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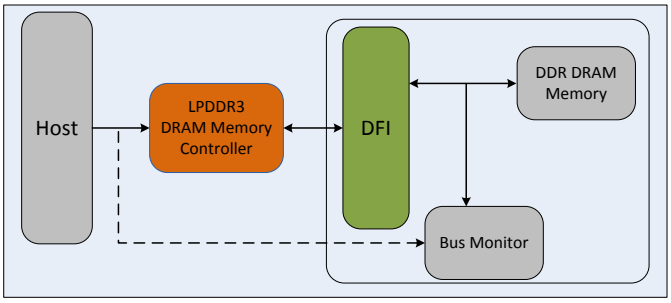
Usage Model:



Value Proposition:

- Will be customized as per Customers' design requirements
- Customized System interface that fits into Customers' need
- Solution delivered completely integrated and validated with targeted PHY - ***(Optional)***
- LPDDR3/4 Joint Solution also available - ***(Optional)***
- Valuable add-on cores such as AHB/AXI, TRR, APB testbus available - ***(Optional)***
- Supports upto 8 system host interfaces
- Programmable Priority/QoS based system bus interface
- Optimized for minimum ASIC gate count
- Flexible licensing models
- Expert Technical support with maintenance updates

Applications:

- Extended battery life makes LPDDR3 to be a choice of memory for consumer devices such as Smartphone, Tablet, Ultrabook
- Other Handheld mobile devices such as Gaming Consoles

Deliverables:

- Synthesizable Source code
- SDC & UPF Constraint details
- UserGuide and Release notes
- Automatic Core maintenance updates
- Verification Components available upon request